IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-8 (canceled)

Claim 9 (original): A method for making a semiconductor device comprising:

forming a first polysilicon layer, which is bracketed by a pair of sidewall spacers, on a first gate dielectric layer, and a p-type polysilicon layer on a second gate dielectric layer;

removing the first polysilicon layer to generate a trench that is positioned between the pair of sidewall spacers;

forming an n-type metal layer within the trench; and

converting substantially all of the p-type polysilicon layer to a silicide.

Claim 10 (original): The method of claim 9 wherein the first gate dielectric layer and the second gate dielectric layer each comprise silicon dioxide, and wherein the first polysilicon layer and the p-type polysilicon layer are each between about 100 and about 2,000 angstroms thick.

Claim 11 (original): The method of claim 9 wherein a wet etch process that is selective for the first polysilicon layer over the p-type polysilicon layer is applied to remove the first polysilicon layer.

Claim 12 (original): The method of claim 9 wherein the n-type metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and wherein all of the p-type polysilicon layer is converted to a silicide.

Claim 13 (original): A method for making a semiconductor device comprising:

forming an n-type polysilicon layer, which is bracketed by a pair of sidewall spacers, on a first gate dielectric layer, and a p-type polysilicon layer on a second gate dielectric layer;

applying a wet etch process that is selective for the n-type polysilicon layer over the p-type polysilicon layer to remove the n-type polysilicon layer without removing significant portions of the p-type polysilicon layer, generating a trench that is positioned between the pair of sidewall spacers, and exposing the first gate dielectric layer;

removing the exposed first gate dielectric layer;

forming a high-k gate dielectric layer on the substrate at the bottom of the trench;

forming an n-type metal layer on the high-k gate dielectric layer to generate a metal NMOS gate electrode; and

converting the p-type polysilicon layer to a silicide to generate a silicide PMOS gate electrode.

Claim 14 (original): The method of claim 13 wherein:

the high-k gate dielectric layer is formed by atomic layer chemical vapor deposition, and comprises a material selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate;

the n-type metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide; and

the silicide comprises a material selected from the group consisting of nickel silicide, cobalt silicide, and titanium silicide.

Claim 15 (original): The method of claim 13 wherein the wet etch process comprises exposing the n-type polysilicon layer to an aqueous solution that includes between about 2 and about 30 percent of a source of hydroxide by volume.

Claim 16 (original): The method of claim 15 wherein the source of hydroxide comprises a compound that is selected from the group consisting of ammonium hydroxide and tetramethyl ammonium hydroxide.

Claims 17-20 (canceled)